WHAT IS CLAIMED IS

1. A testing architecture for a semiconductor memory device, used for testing the semiconductor memory device, the testing architecture comprising:

a microprocessor, wherein when a start signal is received by the microprocessor, a clock signal is output from the microprocessor and transmitted to the semiconductor memory device so that a data storing signal is output from the semiconductor memory device to the microprocessor, wherein when the data storing signal is received by the microprocessor, the data storing signal is tested, compared, and a testing result signal is output; and

a result sorting and display, used to output the start signal to the microprocessor, receive the result signal, and sort the result signal so as to display whether data stored by the semiconductor memory device is correct.

2. The testing architecture of the semiconductor memory device according to claim 1, wherein the microprocessor has a function of receiving serial data, and testing and comparing the data.

3. The testing architecture for the semiconductor memory device according to claim 2, wherein the microprocessor comprises an 8051 integrated circuit (IC).

4. A testing architecture for a semiconductor memory device, used for testing the semiconductor memory device, the testing architecture comprising:

a microprocessor, wherein when a start signal is received by the microprocessor, a clock signal is output from the microprocessor and transmitted to the semiconductor memory device so as to output a data storing signal in series from the semiconductor memory device to the microprocessor, wherein when the data storing signal is received in series by the microprocessor, the data storing signal is tested, compared, and a testing

result is output through a result signal; and

a result sorting and display device, used to output the start signal to the microprocessor, receive the result signal, and sort the result signal so as to display if data stored by the semiconductor memory device is correct.

5. The testing architecture of the semiconductor memory device according to claim 4, wherein the microprocessor comprises an 8051 integrated circuit (IC).